

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yasuhito SUZUKI, et al.

Serial No.: 09/915,366

Filed: July 27, 2001

For: SEMICONDUCTOR PACKAGE AND SEMICONDUCTOR DEVICE

THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231



Group Art Unit: 2811

Examiner: Quang D. Vu

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Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

No additional fee is required.
 Applicant is entitled to small entity status under 37 CFR 1.27
 Also attached: Request for Approval of Drawing Amendment

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	13	20	0	\$18.00 =	\$0.00
Independent Claims	3	3	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
					\$0.00
Total of Above Calculations					\$0.00

Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Date: October 16, 2002



Docket No.: 50090-309

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G/A
P. Walk
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Yasuhito SUZUKI, et al. :
Serial No.: 09/915,366 : Group Art Unit: 2811
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For: SEMICONDUCTOR PACKAGE AND SEMICONDUCTOR DEVICE

AMENDMENT UNDER 37 C.F.R. 1.111

Commissioner for Patents
Washington, DC 20231

Sir:

In response to the July 18, 2002 non-final Office Action, please amend the above-identified application as follows:

IN THE DRAWINGS:

Please amend Figure 4 as shown in the attached Request for Approval of Drawing Amendment.

IN THE CLAIMS:

Please amend/replace claim 9 with the following:

A1 contd B' Sub 97 (Amended) A semiconductor device comprising:
a printed wiring board; and
a plurality of semiconductor packages mounted on the printed wiring board, each semiconductor package having an upper surface of a sealing member thereof facing the printed